A 2V, 2.3/4.6 GHz Dual-Band CMOS Frequency Synthesizer

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Abstract — **This paper describes the design of a CMOS frequency synthesizer for 2.3/4.6 GHz wireless applications. This synthesizer provides dual band output signals by means of a novel frequency doubling technique. Output frequency of the proposed synthesizer ranges from 1.87 GHz-2.3 GHz and 3.74 GHz-4.6 GHz. Fabricated in a 0.35 μm CMOS process, this chip consumes a total power of 80 mW from a single 2 V supply. Chip size is 3210μm x 2410 μm.**

I. INTRODUCTION

With the explosive demands of portable communication devices, CMOS RF front-end ICs have drawn tremendous research efforts in recent years owe to their superiority in low cost and monolithic system integration [1]-[4]. In wireless transceiver, frequency synthesizer provides a local carrier for up-and down frequency conversion. It has a far-reaching influence on overall system SNR, and in general is the key device that dominates power consumption of receiver analog front-end circuits. Major design issues are focused on low noise, low power, frequency resolution, and switching speed.

PLL-based frequency synthesizer is often utilized for RF local oscillator design for it's capable of operating at high speed. Synthesizers of this type can vary their output frequency by changing the divide ratio of the frequency divider in the feedback path. As long as the increasing demands of transmitting bandwidth have pushed the radio frequency of next generation wireless transceivers to be higher than 5 GHz. Meanwhile, the operating speed of voltage-controlled oscillator and frequency divider in the PLL-based frequency synthesizer should be increased as well, which in general results in high power consumption of the radio transceiver.

Fig 1 shows the proposed frequency synthesizer architecture for a 2.3/4.6 GHz dual band wireless application. This synthesizer consists of a voltage controlled oscillator (VCO) that employs an on-chip tuning scheme, a programmable frequency divider (1/N) with a divide ratio ranging from 128 to 65535, a phase-frequency detector (PFD), a 2nd order charge pump loop filter (CP), and a frequency doubler (x 2). The VCO provides quadrature output phases for image rejection down conversion mixers. In addition, high frequency output at 4.6 GHz is indirectly synthesized by means of the frequency doubler. Thereafter, the operating speed of prescaler and VCO can be relaxed, and lower power consumption can be benefited [5]. Moreover, every circuit blocks in the PLL are designed with emphasis on low noise and low voltage operation.

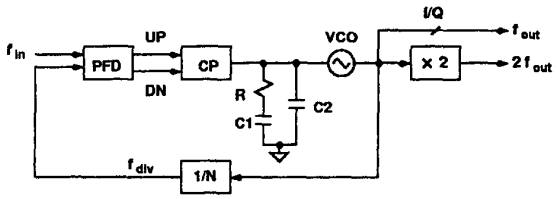

Figure 1. Frequency synthesizer architecture

II. VOLTAGE CONTROLLED OSCILLATOR

Voltage controlled oscillator (VCO) is a key component for PLL-based frequency synthesizer design. Major design considerations include phase noise performance and frequency tuning range. For RF transceiver applications, LC type oscillator is a superior candidate for the inherent bandpass filtering of LC resonator can suppress side-band noise. Conventionally, VCO's output frequency is varied by tuning on-chip varactor diodes. For a multi-GHz range application, varactor diodes should exhibit low parasitic capacitance and wide tuning range to cope with process variations. However, wide-tuning range is difficult to achieve under low supply voltage.

In this paper, a LC voltage controlled oscillator incorporates two mutually-coupled fixed frequency oscillators is adopted [6]. Fig 2 shows the circuit schematic of the VCO, which consists of two identical oscillators, OSC1 (M1, M2, M9, L1, L2) and OSC2 (M5, M6, M12, L3, L4). These two oscillators are mutually coupled by two differential amplifiers (M3, M4, M10) and (M7, M8, M11), and the coupling coefficient is determined by the current source M14. As OSC's close loop phase response is varied by adjusting the weighting of mutual coupling, VCO's output frequency can be changed accordingly [6]. Thus no on chip varactor is required, and VCO's output frequency can be varied by tuning the biased voltage Vfc.

When the two oscillators are frequency syncronized, quadrature output phases can be derived at (I ,$\bar{I}$,Q ,$\bar{Q}$). In order to avoid loss of coupling at the

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extreme case of frequency tuning, an extra current source Idm is added in parallel to M14. Thus, quadrature output phases can be maintained at any output frequency.

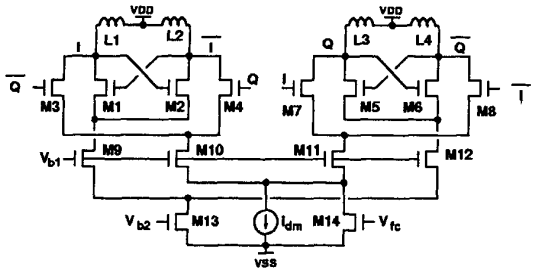

Figure 2. VFO Circuit Schematic

When the quadrature output phases are evenly distributed, the summation of OSC1 and OSC2 switching current should approximate a constant current. Therefore, in this design, OSC1 together with OSC2 are biased at a constant current source M13. This becomes another constraint for quadrature phases at VCO output. Thus, output phase matching can be improved, which is a critical issue in the application of image rejection mixer and frequency doubler. Fig 3 illustrates the simulated VCO output spectrum (A) without and (B) with the current source M13. It reveals that the phase noise performance of the VCO can also be drastically improved when the two OSCs are biased by a constant current source.

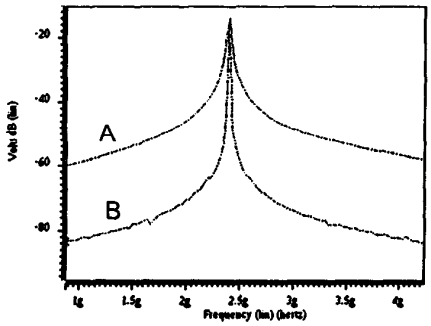

Figure 3. Simulated VCO output spectrum
(A) without (B) with cascode current source M13

The frequency doubler circuit is depicts in Fig 4. By means of I/Q phase mixing, turn on time of the differential amplifier is chopped to $\pi/4$ of the input period, which results in double frequency at the output. The AND functions of the quadrature phases are decomposed into 4 pass transistor logic in parallel, and swapped connected to balance the loading effects from VCO. In this design, inductive loads (L1, L2) of the frequency doubler are made up of bonding wires, and perform as a resonator in cooperation with parasitic capacitance at the output node. This provides band-pass filtering to suppress spurious tones caused by phase mixing.

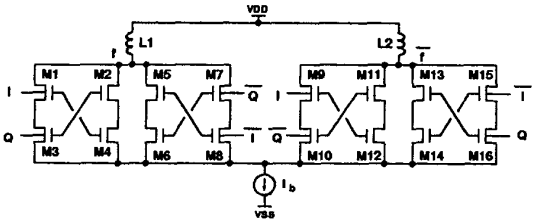

Figure 4. Frequency doubler

II. MULTI-MODULUS FREQUENCY DIVIDER

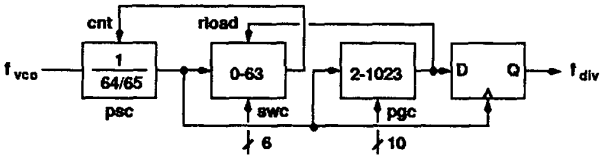

Figure 5. Multi-modulus frequency divider architecture

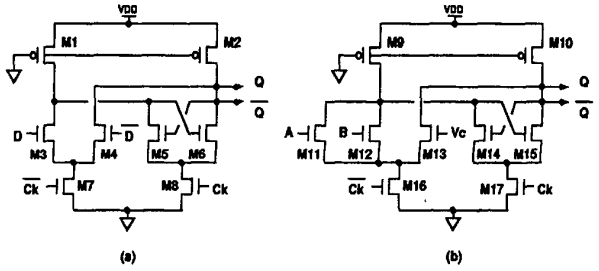

Figure 6. (a) D-Latch (b) D-latch with OR function

Fig 5 shows the architecture of the programmable divider, which consists of a divide by 64/65 prescaler (psc) followed by a 10 bit programmable counter (pgc) and a 6 bit swallow counter (swc). Divide ratio ranges from 128 to 65535. In additon, asynchronous counters are employed in this design for power scaling. To remove accumulated phase errors caused by asynchrounous operations, a resynchronous D flip-flop at the output stage is also adopted [7].

The prescaler is comprised of current mode D-latch, as shown in Fig 6 (a) [8]. The current steering devices M7

and M8 are biased at the boundary of saturation region for high speed operation. Fig 6 (b) shows the D-latch with OR function. The other input of the preamplifier is biased at the common mode voltage of inputs A and B. This architecture reduces circuit complexity and accelerates current switching under low voltage operation.

III. PHASE FREQUENCY DETECTOR AND CHARGE PUMP LOOP FILTER

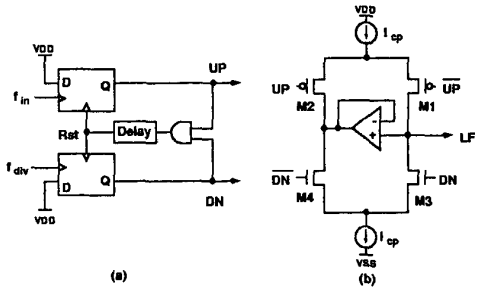

Figure 7. Circuit schematic of (a) phase frequency detector and (b) charge pump.

The phase frequency detector and charge pump loop filter are shown in Fig 7 (a) and (b) respectively. To improve phase resolution, a delay cell is inserted in the feedback path of the tri-state PFD. Thus the minimum turn on time of the charge pumping circuit can be extended. The charge pump circuit is of current steering architecture for high speed and high resolution operation, and the pumping currents are generated from a cascode current source to reduce current mismatches. Moreover, a unity-gain buffer is used to clamp the terminal voltages of current sources during the zero-current pumping period. Thereafter, voltage glitches on the loop filter due to charge sharing can be eliminated [9].

A 2nd order on chip loop filter is designed to suppress the reference spurs. The resistor in loop filter is made up of CMOS transmission gate, and the capacitors are made up of accumulation-mode MOS capacitors. Compared to their inversion or depletion mode counterparts, accumulation mode capacitors manifest better frequency response at high frequency operation. This would stabilize the loop performance for spurs suppression.

IV. EXPERIMENTAL RESULTS

The frequency synthesizer is designed to provide 2.3 GHz and 4.6 GHz dual band output for wireless transceiver application. Figure 8 shows the measured VCO frequency transfer characteristic. Output frequency of the VCO ranges from 1.87 GHz to 2.3 GHz and 3.74 GHz to 4.6 GHz. The conversion gain is about 430 MHz/V.

The measured output spectrum at 2.33 GHz is shown in Fig 9, while the frequency doubler output signal at 4.66 GHz is shown in Fig 10. The measured phase noise at 5 MHz offset are -114 dBc/Hz and -100 dBc/Hz respectively. The spurious free dynamic range at the freuency doubler output is about 48 dB.

The measured PLL dynamic behavior is shown in Fig 11. When the output frequency is hopping from 4.3 GHz to 4.4 GHz, the switching time from 10% to 90% frequency step is less than 60 μ sec, and the settling time within 500 kHz accuracy is about 420 μ sec.

Fig 12 shows the chip photograph of the frequency synthesizer, including a quadrature VCO, an on-chip loop filter, a frequency doubler, a programmable divider, and dual-band output buffers. Implemented in a 0.35 μm digital CMOS process, chip size is about 3210 μm x 2410 μm. Under a single 2 V supply, this chip drains a total power of 80 mW, including 45 mW for output buffer at 2.3 GHz and 4.6GHz.

V. CONCLUSION

This paper describes the design of a single chip 2.3/4.6 GHz dual band frequency synthesizer. In this design, a VCO composed of two identical oscillators is utilized. Frequency tuning is achieved by varying mutual coupling of the two fixed frequency oscillators, thus no on chip varactor is required. This frequency tuning scheme manifests a wide tuning range to overcome temperature and process variation. Moreover, quadrature output phases can be derived from the VCO. And finally, a novel frequency doubler is proposed in this design, which relaxes the operating speed of VCO and prescaler. Thus lower power consumption can be achieved. Doubled frequency output is indirectly synthesized by quadrature phase mixing. The inherent band-pass filtering of the frequency doubler can suppress the spurious tones caused by phase mixing.

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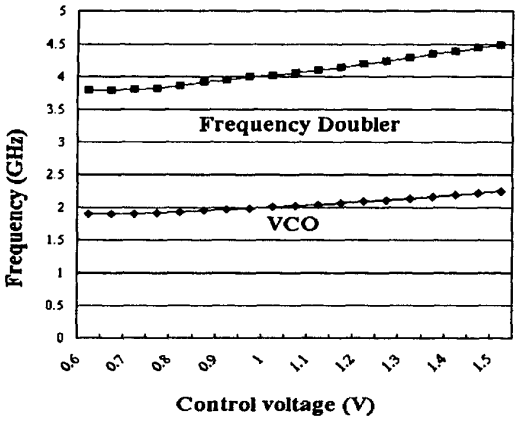

Figure 8. Measured VCO frequency transfer characteristic

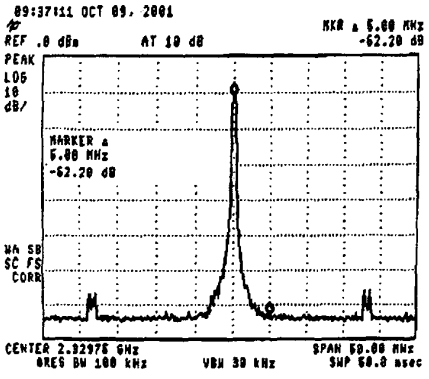

Figure 9. VCO's output spectrum at 2.33 GHz

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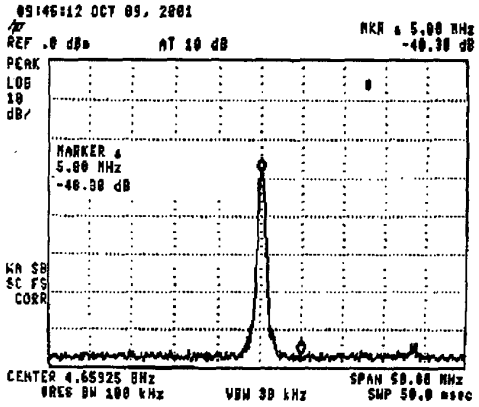

Figure 10. VCO's output spectrum at 4.66 GHz

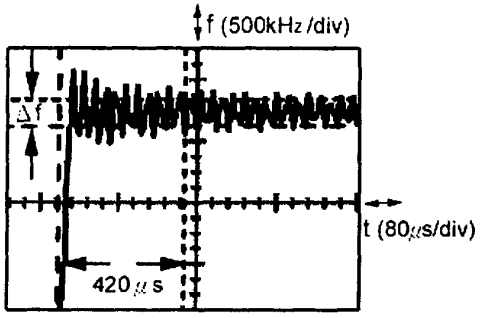

Figure 11. PLL dynamic behavior ($\Delta f = 500$ kHz)

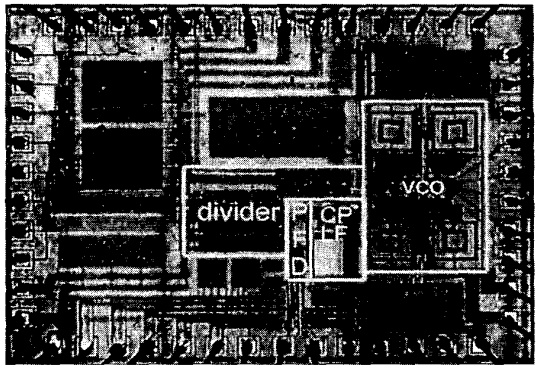

Figure 12. Frequency synthesizer chip micrograph